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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/913,372	11/27/2001	Satoshi Maezawa	MAT8165US	9003

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EXAMINER
PATEL, ISHWARBHAI B

ART UNIT	PAPER NUMBER
2827	

DATE MAILED: 11/06/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	09/913,372	MAEZAWA ET AL.
	Examiner	Art Unit
	Ishwar (I. B.) Patel	2827

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-34* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-34* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 November 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Drawings

1. The drawings are objected to because the figures are improperly cross hatched. All of the parts shown in section, and only those parts, must be cross hatched. The cross hatching pattern should be selected from those shown on page 600-81 of the MPEP based on the material of the part. See also 37 CFR1.84(h)(3) and MPEP 608.02.

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-10 are rejected under 35 U.S.C. 102(b) as being anticipated by Chong et al., US Patent 5,699,613, hereafter Chong.

Regarding claim 1, Chong discloses a multiplayer printed wiring board comprising:

an inner layer material comprising an insulating substrate, a plurality of inner conductive patterns, each of said plurality of inner conductive patterns formed of a metal foil disposed on both sides of said insulating substrate, respectively, and an interstitial via hole disposed on said insulating substrate (base or core laminate of multiple epoxy filled clothe layers 1, patterns 11 and 13 on front and back and via 16, see figure 7, column 3, line 65 to column 4, line 20); and

an insulating resin disposed on both sides of said inner layer material, respectively; an outer conductive pattern adhered on said insulating resin; and a surface via hole to connect electrically between said inner conductive pattern and said outer conductive pattern (dielectric 23, via 31 and pattern 36, see figure 5 and 7, column 4, line 50 to column 5 line 15), wherein

said interstitial via hole connects electrically between respective inner conductive pattern of said plurality of inner conductive pattern, and said outer conductive pattern is formed of a metal foil of a metal foil with insulating resin, said metal foil with insulating resin comprising said insulating resin and said metal foil adhered to said insulating resin (see figure 7).

Regarding claim 2, Chong further discloses the interstitial via hole filled with conductive paste (the hole at 16 is filled with conductive, plateable and solderable polymer 18, column 4, line 5-20).

Regarding claim 3, Chong further discloses a surface via hole with metal plating in said non-through hole (plating 31, see figure 5).

Regarding claim 5, Chong further discloses epoxy resin for both core layer and the dielectric material, column 3, line 65-67 and column 4, line32-48).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 4 and 6-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chong et al., US Patent 5,699,613, hereafter Chong, as applied to claims 1-3 above.

Regarding claim 4, though Chong is not disclosing another layer of plaiting on the outer conductive pattern, applying such additional conductive layer is known in the art for getting the desired thickness on the pattern suitable for the specific requirement or to provide additional plating of noble metal for protecting the outer patterns from the environmental damage. Further, Chong discloses such additional plating for the inner layer, see figure 3B, column 4, line 20-30. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to provide the circuit

board of Chong with metal plating on the surface of conductive pattern for outer layer in order to protect the outer layer from environmental damage.

Regarding claims 6 and 7, the applicant is claiming the resin in insulator is thermosetting resin and the base material is formed of aromatic polyamide with porous structure as claimed in claim 6 and the base material has a nonwoven fabric formed of aromatic polyamide fibers. Though, Chong is not disclosing such material for insulating base, such materials are known in the art and can be used depending upon specific requirement. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to provide the circuit board of Chong with the material as claimed in order to get the desired end results, since it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use as a matter of obvious design choice. *In re Leshin*, 125 USPQ 416.

Regarding claim 8, though Chong is not disclosing the non through hole in the range of from about 30 μm to about 100 μm, the crux of the invention of Chong is to increase the component density by decreasing the via diameter. Further, Chong discloses via diameters nominally 0.12 millimeters or less, which is about 120 μm or less, column 2, line 1-10.

Regarding claim 9, though Chong is not disclosing non through hole formed by lesser beam machining, the laser beam machining is known in the art for precise drilling of a hole and can be used depending upon specific requirement. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to provide the circuit board of Chong with the holes made by laser beam machining in order to have precise control of the hole drilling.

Regarding claim 10, though Chong is not disclosing plurality of insulating substrates, the multilayer boards with plurality of layers is known in art for increasing the component density with desired power / ground / signal layers. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to provide the circuit board of Chong with the inner layer material comprising plurality of insulating substrates in order to increased component density with desired power / ground / signal layers.

6. Claims 11-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chong et al., US Patent 5,699,613, hereafter Chong, as applied to claims 1-10 above, and further in view of Yamamoto et al., US Patent 5,736,681, hereafter Yamamoto.

Regarding claim 11, Chong discloses all the features of the claimed invention as applied to claims 1-10 except the conductor projection connected electrically with said inner conductive patterns. However, such conductor projection for electrical connection

between two layers of a printed circuit board is known in the art. Yamamoto discloses such conductor projection for electrical and thermal conductivities between the wiring patterns. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to provide the circuit board of Chong with conductor projection connected electrically with said inner conductive patterns in order to have electrical and thermal conductivities between the wiring patterns.

Regarding claim 12, the modified circuit board of Chong further discloses the insulating substrate formed of sheet like resin preprag, Yamamoto, column 15, line 5-15.

Regarding claim 13, though the modified assembly of Chong is not disclosing non through hole formed by lesser beam machining, the laser beam machining is known in the art for precise drilling of a hole and can be used depending upon specific requirement. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to provide the modified circuit board of Chong with the holes made by laser beam machining in order to have precise control of the hole drilling.

Regarding claim 14, the modified circuit board of Chong further discloses the projection formed of a conductive paste, Yamamoto, column 11, line 29-35.

Regarding claim 15, the modified circuit board of Chong further discloses the conductor projection in the shape of a cone, see Yamamoto figure 5-6.

Regarding claim 16, the modified circuit board of Chong further discloses a surface via hole with metal plating in said non-through hole (Chong, plating 31, see figure 5).

Regarding claim 17, though the modified circuit board of Chong is not disclosing another layer of plaiting on the outer conductive pattern, applying such additional plating layer is known in the art for getting the desired thickness on the pattern suitable for the specific requirement or to provide additional plating of noble metal for protecting the outer patterns from environmental damage. Further, Chong discloses such additional plating for the inner layer, see figure 3B, column 4, line 20-30. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to provide the modified circuit board of Chong with metal plating on the surface of conductive pattern for outer layer in order to protect the outer layer from environmental damage.

Regarding methods claims 18-34, the method claims are obvious in view of the product claims 1-17.

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Odaira et al, Card, Jr., et al., Yamamoto et al., Hayashi et al., Schmidt, Motomura et al., Echigo et al., Akishi et al., Jiro et al., and Shoji et al., discloses circuit board similar to applicant's claimed invention.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ishwar (I. B.) Patel whose telephone number is (703) 305 2617. The examiner can normally be reached on M-F (6:30 - 4) First Friday Off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David L Talbott can be reached on (703) 305 9883. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 305 3431 for regular communications and (703) 305 7724 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308 0956.

Albert W. Paladini 11-2-01

ALBERT W. PALADINI
PRIMARY EXAMINER

ibp
October 25, 2002